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AGILENT TECHNOLOGIES, INC.
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Kirt Reed Williams

Serial No.: 10/668,136

Examiner: Parekh, Nitin

Filing Date: September 22, 2003

Group Art Unit: 2811

Title: SEMICONDUCTOR STRUCTURE WITH ELECTRICALLY ISOLATED SIDEWALL ELECTRODES AND METHOD FOR FABRICATING THE STRUCTURE

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Sir:

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on October 5, 2005

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) **$500.00**.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

☐ (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)(1)-(5)) for the total number of months checked below:

☐	one month	$ 120.00
☐	two months	$ 450.00
☐	three months	$1020.00
☐	four months	$1590.00

☐ The extension fee has already been filled in this application.

☒ (b) Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account **50-1078** the sum of $500.00. At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account **50-1078** pursuant to 37 CFR 1.25.

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☐ I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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☒ I hereby certify that this paper is being facsimile transmitted to the Patent and Trademark Office on the date shown below.

Date of Facsimile: December 5, 2005

Typed Name: Thomas H. Ham

Signature: Thomas H. Ham

Respectfully submitted,

Kirt Reed Williams

By Thomas H. Ham

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Date: December 5, 2005

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Attorney Docket No. 10010900-1 PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Kirt Reed Williams
Group Art Unit: 2811
Serial No. 10/668,136
Confirmation No. 2011
Filed: September 22, 2003
Examiner: Parekh, Nitin

For: SEMICONDUCTOR STRUCTURE WITH ELECTRICALLY ISOLATED SIDEWALL ELECTRODES AND METHOD FOR FABRICATING THE STRUCTURE

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

BRIEF ON APPEAL

Sir/Madam:

This brief is in furtherance of Applicants' Notice of Appeal filed on October 5, 2005, appealing the decision of the Examiner dated July 15, 2005 finally rejecting claims 1-15.

CERTIFICATE OF TRANSMISSION UNDER 37 C.F.R. 1.8

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being facsimile transmitted to the Patent and Trademark Office facsimile number (571) 273-8300 on December 5, 2005.

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Typed Name: Thomas H. Ham

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I. Real Party in Interest

The real party in interest in this appeal is Agilent Technologies, Inc., a Delaware Corporation, having a place of business at 395 Page Mill Road, Palo Alto, California 94303.

II. Related Appeals and Interferences

There are currently no related appeals or interference proceedings in progress that will directly affect, or be directly affected by, or have a bearing on the Board's decision in the present Appeal.

III. Status of Claims

Claims 1-23 were originally filed with the application on September 22, 2003. In Response to Office Action filed on July 28, 2004, claims 1-15 were elected in response to a restriction requirement. As a result, claims 13-20 were withdrawn from consideration. In the Amendment and Response to Office Action filed on May 12, 2005, claim 10 was amended. No claims have been amended, canceled, or added for purposes of this Appeal.

Claims 1-15 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over U.S. Patent No. 5,888,884 ("Wojnarowski") in view of U.S. Patent No. 6,201,631 ("Greywall").

This Appeal is made with regard to pending claims 1-15.

IV. Status of Amendments

No amendments were filed subsequent to final rejection.

V. Summary of Claimed Subject Matter

The claimed invention is a semiconductor structure with electrically isolated sidewall electrodes on one or more sides of the structure and a method for fabricating the structure (see Applicant's specification on page 3, lines 3-5). According to an embodiment of the invention, as recited in claim 1, a semiconductor structure comprises a semiconductor core (112) having a side surface (106, 108), a layer (114; 514) of insulating material on the side surface, and electrically isolated electrodes (110; 510) arrayed along the layer of insulating material on the side surface. The electrically isolated electrodes include a conductive material having etch selectivity with respect to the insulating material. According to an embodiment of the invention, as recited in claim 10, a semiconductor structure comprises a semiconductor core (112) having a major surface (102) and a side surface (106, 108), the major surface being orthogonal to the side surface, a continuous layer (114; 514) of insulating material on the side surface, and electrically isolated electrodes (110; 510) arrayed along the continuous layer of insulating material on the side surface such that the electrically isolated electrodes extend substantially in a direction orthogonal to the major surface. The electrically isolated electrodes include conductive material having etch selectivity with respect to the insulating material.

VI. Grounds of Rejection to be Reviewed on Appeal

Whether claims 1-15 are unpatentable under 35 U.S.C. 103(a) over Wojnarowski in view of Greywall.

VII. Argument

A. Rejection of Independent Claims 1 and 10 Under 35 U.S.C. §103(a)

The independent claims 1 and 10 were rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Wojnarowski in view of Greywall.

However, the Examiner has failed to establish a *prima facie* case of obviousness under 35 U.S.C. §103(a) for claims 1 and 10. To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

In the case at hand, there is no valid suggestion or motivation to combine the teachings of Wojnarowski and Greywall, as asserted by the Examiner. In addition, there is no reasonable expectation of success to combine the teachings of Wojnarowski and Greywall. Furthermore, the cited references of Wojnarowski and Greywall when combined do not teach or suggest all of the limitations of either claim 1 or 10. Thus, the Examiner has failed to establish a *prima facie* case of obviousness for claims 1 and 10.

i. <u>There is no valid suggestion or motivation to combine the teachings of Wojnarowski and Greywall</u>

There is no valid suggestion or motivation to combine the teachings of Wojnarowski and Greywall to derive the claimed invention, as recited in claims 1 and 10. On page 5 of the Final Office Action of July 15, 2005, the Examiner correctly states that "Wojnarowski fails to teach the conductive material having etch selectivity with respect to the insulating material." However, the Examiner then asserts that "Greywall teaches using the DRIE process to etch conventional electrode/conductive material including polysilicon where an etchant has etch selectivity with respect to oxide/insulating material (Fig. 4 and 5; Col. 5, lines 30-65; Col. 6, lines 35-45)." In order to provide some sort of suggestion or motivation to combine the teachings of Wojnarowski and Greywall, the Examiner

then asserts that "[s]uch conductive structure and etch process provides an improved metal removal/etch and profile, reduced undercut and improved HDI reliability."

However, there is no suggestion or motivation found in the cited references of Wojnarowski and Greywall to make the combination asserted by the Examiner. In fact, the cited teaching of Greywall with respect to DRIE has nothing to do with electrodes, let alone "*electrically isolated electrodes arrayed along said (continuous) layer of insulating material on said side surface*," as recited in claims 1 and 10. Thus, the cited reference of Greywall does not provide a suggestion or motivation to combine the teachings of Wojnarowski and Greywall.

The cited passage of Greywall in column 5, lines 30-65, describes that DRIE can be used to form cavities 9 in the bottom silicon layer 50 of a silicon-oxide-silicon substrate. However, the cited passage of Greywall in column 6, lines 35-45, which describes electrodes and interconnects, has nothing to do with DRIE. Consequently, the two cited passages of Greywall are not related with respect to DRIE. Thus, Greywall only discloses using DRIE to form cavities 9 in the bottom silicon layer 50, not "*electrically isolated electrodes arrayed along said (continuous) layer of insulating material on said side surface*," as recited in claims 1 and 10. Since Greywall discloses using DRIE to form only cavities in a bottom silicon layer of a silicon-oxide-silicon substrate, Greywall does not provide a motivation or suggestion to combine the teaching of Greywall with the teaching of Wojnarowski to derive the claimed invention, as recited in claims 1 and 10. Therefore, there is no valid suggestion or motivation found in the cited references of Wojnarowski and Greywall to combine the teachings of Wojnarowski and Greywall to derive the claimed invention, as recited in claims 1 and 10.

The only "motivation" for combining the teachings of Wojnarowski and Greywall is the rationale set forth by the Examiner, which is not supported by the cited references. Therefore, the Examiner has failed to provide a valid suggestion

or motivation to combine the teachings of Wojnarowski and Greywall to establish a *prima facie* case of obviousness for claims 1 and 10.

ii. There is no reasonable expectation of success to combine the teachings of Wojnarowski and Greywall

There is no reasonable expectation of success to combine the teachings of Wojnarowski and Greywall to derive the claimed invention, as recited in claims 1 and 10. As admitted by the Examiner on page 5 of the Final Office Action of July 15, 2005, "Wojnarowski fails to teach the conductive material having etch selectivity with respect to the insulating material." Thus, the cited reference of Wojnarowski does not provide a reasonable expectation of success to combine the teachings of Wojnarowski and Greywall to derive the claimed invention, as recited in claims 1 and 10. However, the Examiner further states on page 5 of the Final Office Action of July 15, 2005 that "Greywall teaches using the DRIE process to etch conventional electrode/conductive material including polysilicon where an etchant has etch selectivity with respect to oxide/insulating material (Fig. 4 and 5; Col. 5, lines 30-65; Col. 6, lines 35-45)."

As stated above, the cited reference of Greywall discloses using DRIE to form cavities 9 in the bottom silicon layer 50, not "*electrically isolated electrodes arrayed along said (continuous) layer of insulating material on said side surface*," as recited in claims 1 and 10. Thus, Greywall does not teach the limitation of "*said electrically isolated electrodes including a conductive material having etch selectivity with respect to said insulating material*," as recited in claims 1 and 10. Since the cited reference of Greywall only discloses using DRIE to form cavities in a silicon layer, the Greywall does not provide a reasonable expectation of success to combine the teachings of Wojnarowski and Greywall to derive the claimed invention, as recited in claims 1 and 10.

iii. Cited references of Wojnarowski and Greywall when combined do not teach or suggest all of the limitations of claims 1 and 10

The cited references of Wojnarowski and Greywall when combined do not teach or suggest all of the limitations of claims 1 and 10. The independent claim 1 recites in part "*electrically isolated electrodes arrayed along said layer of insulating material on said side surface.*" Similarly, the independent claim 10 recites in part "*electrically isolated electrodes arrayed along said continuous layer of insulating material on said side surface.*" In the Final Office Action on page 3, the Examiner alleges that Wojnarowski discloses "a plurality of electrically isolated and patterned electrodes/channels arrayed along the continuous layer of the insulating material on the side surfaces including each left and right side surface (see one of the plurality of 62/64, shown as being connected with respective one of the plurality of interconnects/pads 40 on each side surface in Fig. 8; Col. 6, lines 37-43; Col. 7, lines 49-65; also see Col. 7, lines 63-65)." However, the cited reference of Wojnarowski in fact does not disclose such "electrically isolated and patterned electrodes/channels."

In Fig. 8 of Wojnarowski, "hole" metallizations 62 that are connected to bottom pads 64 are shown. Each hole metallization 62 is on a particular layer of insulating material 54. The layers of insulating material 54 are shown and identified in Figs. 3-5 and 7, but not identified in Figs. 6 and 8. Each of these metallizations 62 is not on the same layer of insulating material, but rather on a different layer of insulating material. Consequently, Wojnarowski does not disclose "*electrically isolated electrodes arrayed along said (continuous) layer of insulating material on said side surface,*" as recited in claims 1 and 10.

As illustrated in Figs. 1-7 and described in the specification of Wojnarowski, each hole metallization 62 on a particular layer of insulating material 54 is formed in the following manner. First, holes 50 are formed through a wafer 30 (See Fig. 2; column 6, lines 64-65). Next, an insulating coating 54 is formed on all exposed surfaces of the wafer 30, including the top surface 32, the bottom surface 34 and surfaces within the holes 50 (See Fig. 3; column 7, lines

16-18). Opening 56 are then formed in the insulating coating on the top surface 32 to provide access to top interconnection pads 40 (See Fig. 4; column 7, lines 29-31). Next, the wafer 30 is cleaned, backsputtered and metallized on both sides, forming metallization 60 (See Fig. 5; column 7, lines 37-41). Excess metal are then removed using patterned resist, leaving patterned metal 62 (See Fig. 6; column 7, lines 46-53). Next, the wafer 30 is sawed using a dicing saw such that each metallized hole 50 is divided in two, resulting in a half-barrel appearance (See Fig. 7; column 7, lines 54-65). As a result, for each divided "half-barrel" hole 52, one metallization 62 on a single layer of insulating material 54 is formed. Thus, Wojnarowski discloses metallizations 62 on different layers of insulating material 54 such that each metallization is on a particular layer of insulating material. Consequently, Wojnarowski does not disclose "*electrically isolated electrodes arrayed along said (continuous) layer of insulating material on said side surface*," as recited in claims 1 and 10. Therefore, the cited references of Wojnarowski and Greywall when combined do not teach or suggest all of the limitations of claims 1 and 10.

In addition, the cited reference of Wojnarowski, as admitted by the Examiner, and the cited reference of Greywall, as explained above, do not teach the limitation of "*said electrically isolated electrodes including a conductive material having etch selectivity with respect to said insulating material*," as recited in claims 1 and 10. Therefore, the cited references of Wojnarowski and Greywall when combined do not teach or suggest all of the limitations of claims 1 and 10.

Furthermore, the different layers of insulating material 54 of Wojnarowski are not on a side surface of a separated wafer segment 70, but within channels defined by the divided "half-barrel" holes 52. When the wafer 30 is separated using a dicing saw, the side surfaces of the resulting wafer segments, such as the wafer segment 70, are the exposed surfaces between the channels. Since the layers of insulating material 54 are within these channels, the layers of insulating material are not on a side surface, as recited in claims 1 and 10. As a result, the cited reference of Wojnarowski does not disclose "*electrically isolated electrodes*

arrayed along said (continuous) layer of insulating material on said side surface," as recited in claims 1 and 10. Therefore, the cited references of Wojnarowski and Greywall when combined do not teach or suggest all of the limitations of claims 1 and 10.

B. Rejection of Independent Claims 2-9 and 11-15 Under 35 U.S.C. §103(a)

The dependent claims 2-9 and 11-15 were rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Wojnarowski in view of Greywall. However, the Examiner has failed to establish a *prima facie* case of obviousness under 35 U.S.C. §103(a) for these dependent claims 2-9 and 11-15. To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Each of the dependent claims 2-9 and 11-15 depends on one of the independent claims 1 and 10. As such, these dependent claims include all the limitations of their respective base claims. Therefore, the Examiner has also failed to establish a *prima facie* case of obviousness for these dependent claims 2-9 and 11-15 for at least the same reasons as their respective based claims.

SUMMARY

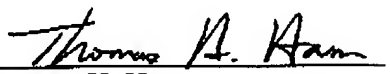
The Examiner has failed to establish a *prima facie* case of obviousness under 35 U.S.C. §103(a) for claims 1-15. The cited references of Wojnarowski and Greywall do not provide a suggestion or motivation to combine the teachings

of Wojnarowski and Greywall. In addition, the cited references of Wojnarowski and Greywall do not provide a reasonable expectation of success to combine the teachings of Wojnarowski and Greywall. Furthermore, the cited references of Wojnarowski and Greywall when combined do not teach or suggest all of the claim limitations. Therefore, claims 1-15 cannot be rendered obvious over Wojnarowski in view of Greywall.

For all the foregoing reasons, it is earnestly and respectfully requested that the Board of Patent Appeals and Interferences reverse the rejections of the Examiner regarding claims 1-15, so that this case may be allowed and pass to issue in a timely manner.

Respectfully submitted,
Kirt Reed Williams

Date: December 5, 2005

By: 
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VIII. Claims Appendix

1. A semiconductor structure comprising:

a semiconductor core having a side surface;

a layer of insulating material on said side surface; and

electrically isolated electrodes arrayed along said layer of insulating material on said side surface, said electrically isolated electrodes including a conductive material having etch selectivity with respect to said insulating material.

2. The semiconductor structure of claim 1 wherein said electrically isolated electrodes extend substantially in a direction orthogonal to a major surface of said semiconductor core, said major surface being orthogonal to said side surface.

3. The semiconductor structure of claim 1 wherein said conductive material includes silicon-based conductive material.

4. The semiconductor structure of claim 3 wherein said silicon-based conductive material includes polysilicon.

5. The semiconductor structure of claim 1 wherein said semiconductor core includes single-crystal silicon.

6. The semiconductor structure of claim 1 wherein said insulating material of said layer includes oxide of said semiconductor core.

7. The semiconductor structure of claim 1 wherein said electrically isolated electrodes are additionally arrayed over a major surface of said semiconductor core, said major surface being orthogonal to said side surface.

8. The semiconductor structure of claim 7 further comprising interconnects electrically connected to selected ones of said electrically isolated electrodes, said interconnects being positioned over said major surface of said semiconductor core.

9. The semiconductor structure of claim 7 wherein said electrically isolated electrodes are additionally arrayed along a second side surface of said semiconductor core.

10. A semiconductor structure comprising:

a semiconductor core having a major surface and a side surface, said major surface being orthogonal to said side surface;

a continuous layer of insulating material on said side surface; and

electrically isolated electrodes arrayed along said continuous layer of insulating material on said side surface such that said electrically isolated electrodes extend substantially in a direction orthogonal to said major surface, said electrically isolated electrodes including conductive material having etch selectivity with respect to said insulating material.

11. The semiconductor structure of claim 10 wherein said conductive material includes silicon-based conductive material.

12. The semiconductor structure of claim 11 wherein silicon-based conductive material includes doped polysilicon.

13. The semiconductor structure of claim 10 wherein said semiconductor core includes single-crystal silicon.

14. The semiconductor structure of claim 10 wherein said electrically isolated electrodes additionally extend over said major surface of said semiconductor core.

15. The semiconductor structure of claim 14 further comprising interconnects electrically connected to selected ones of said electrically isolated electrodes, said interconnects being positioned over said major surface of said semiconductor core.

16. A method for fabricating a semiconductor structure, the method comprising:

providing a semiconductor core with a side surface;

forming a layer of insulating material on said side surface of said semiconductor core;

forming a layer of conductive material adjacent to said layer of insulating material on said side surface, said conductive material having etch selectively with respect to said insulating material; and

selectively etching said layer of conductive material using a stop-on-oxide deep reactive ion etching to define electrically isolated electrodes arrayed along said layer of insulating material on said side surface.

17. The method of claim 16 wherein said selectively etching includes selectively etching said layer of conductive material using said stop-on-oxide deep reactive ion etching such that said electrical isolated electrodes extend substantially in a direction orthogonal to a major surface of said semiconductor core, said major surface being orthogonal to said side surface.

18. The method of claim 16 wherein said forming of said layer insulating material includes forming a layer of oxide on said side surface of said semiconductor core.

19. The method of claim 16 wherein said forming of said layer of conductive material includes forming a layer of silicon-based conductive material adjacent to said layer of insulating material.

20. The method of claim 19 wherein said forming of said layer of silicon-based conductive material includes forming a layer of polysilicon adjacent to said layer of insulating material.

21. The method of claim 16 wherein said providing of said semiconductor core includes providing a single-crystal silicon core with said side surface.

22. The method of claim 16 wherein said forming of said layer of conductive material includes forming said layer of conductive material over a major surface of said semiconductor core, said major surface being orthogonal to said side surface, and wherein said selectively etching of said layer of conductive material includes selectively etching said layer of conductive material over said major surface of said semiconductor core using said stop-on-oxide deep reactive ion etching such that said electrically isolated electrodes extend over said major surface of said semiconductor core.

23. The method of claim 22 further comprising forming interconnects over said major surface of said semiconductor core, said interconnects being electrically connected to selected ones of said electrically isolated electrodes.

IX. Evidence Appendix

NONE

X. Related Proceedings Appendix

NONE